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Muhammad Awais Hussain

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Education

National Central University, Taiwan — PhD in Electrical Engineering
Grade: **90.3%** — **2019-02 ~ 2023-01**

National Central University, Taiwan — MS in Electrical Engineering
Grade: **90.7% (Top 5%)** — **2016-09 ~ 2018-06**

University of Bradford, UK — BS in Electrical Engineering
Grade: **79% (First Class honors)** — **2011-09 ~ 2015-09**

Relevant Skills

Programming and Scripting: Python, Verilog, C, C++, Matlab, TCL, PERL
Tools and Libraries: TestMax Manager, TMAX-II, SMS, VTRAN, VCS, IC Compiler, Synopsys DC, DFTC, Verdi, Matlab, Vivado, Visual Studio, Fastai, PyTorch, Keras

Work Experience

- ***Senior Staff DFT Engineer*** ***SiliconAuto, Taiwan*** ***October 2024-TBD***
  - Responsible for planning, execution, and creation of DFT flows for automotive chips
  - Support test engineers in testing of chips by production and debugging patterns generation
- ***Senior DFT Engineer*** ***Global UniChip (GUC), Taiwan*** ***April 2023 – September 2024***
  - Responsible for DFT flows development and enhancement, and training project teams
  - Completed development and implementation of DFTMAX SEQ, LOES, and RAMSEQ flows
  - Enhanced Tessent/Synopsys ATPG flows for test coverage improvement based on coverage loss
  - Supported project teams to solve DFT-related issues
  - Completed DFTMAX ULTRA and XLBIST based SCAN flow for Automotive project in 5nm
- ***Digital IC Design Intern*** ***Maxense Innovations, Taiwan*** ***April 2022 – April 2023***
  - Developed a new low-power architecture for memory controller and data compression/decompression engine in TDDI for mobile phone and smart-watch
- ***Digital IC Design Intern*** ***Damo Technology, Taiwan*** ***July 2021 – April 2022***
  - Worked on analyzing and improving power-critical blocks in TDDI
  - Improved data compression/decompression engine for low-power consumption
- ***Research Assistant*** ***Namal College, Pakistan*** ***April 2016 – July 2016***
  - Worked on integration of design thinking and TRIZ for prospective engineers
  - Responsibilities included data collection, analysis and sessions with research participants

Projects

- **Incremental Learning on Chip (PhD Research)**
  - Designed an incremental learning chip for efficient, low-power, and high-speed inference and training of fully connected layers using edge-optimized incremental learning algorithm in TSMC 40nm technology. Memory access and storage memory reduction was performed using edge-optimized incremental learning algorithm.
- **Edge-Optimized Incremental Learning Algorithm (PhD Research)**
  - Developed a cutting-edge incremental learning algorithm for edge devices using Fastai, achieving same accuracy performance as state-of-the-art incremental learning algorithms. Collaborated with Industrial Technology Research Institute (ITRI), Taiwan for this work.
- **FBCOT encoding in FPGA (Master Research project)**

- Designed a high throughput and low-power encoder module of Fast Block Coding with Optimized Truncation (FBCOT) used in High Through JPEG 2000 (HTJ2K). Collaborated with University of New South Wales, Australia and University of Stuttgart, Germany for project.

- **ECG compression chip (Master Thesis)**
  - Designed ultra-low power ECG compression chip using TSMC 90nm and 180nm technology. Used Synopsys tools to complete RTL to GDSII flow during development cycle.
- **Blow Fish encryption algorithm in FPGA (Bachelor Project)**
  - Designed hardware implementation of Blow Fish encryption algorithm in FPGA, with the focus on high throughput and low power consumption.

Publications

- **M. A. Hussain**, S. A. Huang and T. H. Tsai, "Learning with Sharing: An Edge-optimized Incremental Learning Method for Deep Neural Networks," in *IEEE Transactions on Emerging Topics in Computing*, 2022
- **M. A. Hussain**, L. C. Lee, and T. H. Tsai, "An Efficient Incremental Learning Algorithm for Sound Classification," in *IEEE Multimedia*, 2022
- **M. A. Hussain**, L. C. Lee, and T. H. Tsai, "An Area-Efficient and High Throughput Hardware Implementation of Exponent Function," in *IEEE ISCAS*, 2022
- **M. A. Hussain** and T. H. Tsai, "Memory Access Optimization for On-Chip Transfer Learning," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2021
- **M. A. Hussain** and T. Tsai, "An Efficient and Fast Softmax Hardware Architecture (EFSHA) for Deep Neural Networks," in *IEEE AICAS*, Online, 2021
- T. H. Tsai and **M. A. Hussain**, "VLSI Implementation of Lossless ECG Compression Algorithm for Low Power Devices," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2020.
- T. H. Tsai, C. Huang, C. Chang and **M. A. Hussain**, "Design of Wireless Vision Sensor Network for Smart Home," in *IEEE Access*, vol. 8, pp. 60455-60467, 2020
- I. Althamary, **M. A. Hussain**, Y. H. Li, "An Improved Framework of Accurate Iris Segmentation under Relaxed Imaging Constraints using Total Variation Model", in *CVGIP*, Taitung, Taiwan, 2019
- T. H. Tsai, **M. A. Hussain**, P. Hao, "VLSI Implementation of ECG Compression Algorithm using Golomb Rice Coding", in *IEEE ICCE-Taiwan*, Taichung, Taiwan, 2018 ***(Best Paper Award)***
- **M. A. Hussain** and R. Badar, "FPGA Based Implementation Scenarios of TEA Block Cipher," in *IEEE FIT*, Islamabad, Pakistan, 2015
- M. Khan, **M. A. Hussain**, K. Chaudry, U. Tauseef, S. Nawaz, and R. Jawad, "A Bi-directional Prototype Mobile Robot to Experiment Light Scale Object-Transportation Schemes", in *IEEE ICET*, Islamabad, Pakistan, 2014

Patents

- U.S. Patent 17406458 "Device, Memory Access Method and Non-Volatile Storage Medium," December, 2022
- Taiwan Patent I769875, "深度學習網路裝置、其使用的記憶體存取方法與非揮發性儲存媒介," July, 2022
- Taiwan Patent 111127482, "用於深度神經網路之邊緣優化增量學習方法與電腦系統," December, 2023

References

- Provided upon request

Extra-curricular Activities

- Gymnasium
- Cooking