Resume

<table>
<tr><td colspan="2">Name</td><td>Awais Hussain</td><td>Advisor</td><td>Tsung-Han Tsai</td><td rowspan="4">  </td></tr>
<tr><td colspan="2">Application for position</td><td colspan="3">Digital IC Design Engineer</td></tr>
<tr><td colspan="2">Address</td><td colspan="3">No. 49, Alley 1, Lane 137, Zheng Guang Street, Zhongli District, Taoyuan City, Taiwan</td></tr>
<tr><td colspan="2">E-Mail</td><td>awais.hussain6@gmail.com</td><td>Mobile No.</td><td>+886-984-389 184</td></tr>
<tr><td rowspan="5">Education</td><td>Academics</td><td>Institute</td><td colspan="2">Department</td><td>Grades</td></tr>
<tr><td>PhD</td><td>National Central University, Taoyuan, Taiwan</td><td colspan="2">Electrical Engineering (2019-2~2023-1)</td><td>90.3%</td></tr>
<tr><td>Master</td><td>National Central University, Taoyuan, Taiwan</td><td colspan="2">Electrical Engineering (2016-9~2018-6)</td><td>90.75%; Position: 7/117 (Top 5%)</td></tr>
<tr><td>Bachelor</td><td>University of Bradford, UK</td><td colspan="2">Electrical Engineering (2011-9~2015-9)</td><td>72% (First class honors)</td></tr>
<tr><td>Senior High School</td><td>F.B.I.S.E, Pakistan</td><td colspan="2">Pre-Engineering (2009-5~2011-5)</td><td>79%</td></tr>
<tr><td colspan="2" rowspan="6">Skill Set</td><td colspan="4">Development of designing and verification flow for VLSI design</td></tr>
<tr><td colspan="4">Frontend (Verilog) and Backend (Physical Design layout) experience</td></tr>
<tr><td colspan="4">Familiarity with Deep Learning Based Computer Vision</td></tr>
<tr><td colspan="4">Familiarity with MIPI DCS, MIPI DSI, MIPI DPI</td></tr>
<tr><td colspan="4">Familiarity with industry-standard circuit design and verification tools, flows and methodologies</td></tr>
<tr><td colspan="4">Superior written and oral English communication skills</td></tr>
<tr><td rowspan="3">Technical Skills</td><td>Programming</td><td colspan="4">C, C++, Verilog, VHDL, Python</td></tr>
<tr><td>CAD tool</td><td colspan="4">Matlab, Xilinx ISE, Xilinx Vivado, Altera Quartus; Visual Studio; Synopsys Design Compiler, Synopsys IC Compiler, Verdi, Siloti</td></tr>
<tr><td>Deep Learning Libraries</td><td colspan="4">Fastai, PyTorch, Keras</td></tr>
<tr><td colspan="2">Projects</td><td colspan="4">1. Learning on Chip (PhD Research)
For PhD research, I have worked on the implementation of incremental learning on chip. This research has helped to perform learning on the edge where low power devices are utilized to perform training on the edge. In the first stage of training Deep Neural Networks (DNNs) on the edge devices, an optimized memory access has been designed that is able to reduce memory access resulting in saving of power consumption on the edge devices.
2. Learning with Sharing: An Edge-Optimized Incremental</td></tr>
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	Learning Algorithm (PhD Research) A new incremental learning algorithm was developed to bring the incremental learning on the edge devices. The algorithm was designed in Fastai. The proposed algorithm is able to achieve the same accuracy performance as state-of-the-art incremental learning algorithms. This work was performed in collaboration with Industrial Technology Research Institute (ITRI), Taiwan. **3. Implementation of FBCOT encoding in FPGA (Master Research)** Fast Block Coding with Optimized Truncation (FBCOT) is new proposed engine for data compression in JPEG2000. The digital hardware design of the encoder module was completed. The main aims of the design were achieving high throughput with minimum resources usage. For this project, collaboration work was performed with Professor David Taubman from University of New South Wales, Australia and a team from University of Stuttgart, Germany. 4. **Designing of ECG compression chip (Master Thesis)** Complete digital design and layout of ECG compression design was performed using TSMC90nm and TSMC0.18um technology. Synthesis of implemented design was done using Design Compiler. Floor planning, placement, clock tree synthesis and routing was completed in IC Compiler. DRC and LVS were performed in Calibre. **5. Automatic Iris segmentation and recognition** Automatic iris segmentation and recognition was performed using total variation model. This project is implemented using Matlab. Main purpose of this project was to increase the speed of segmentation while maintaining highest accuracy. **6. Implementation of Blow Fish encryption algorithm in FPGA (Bachelor Project)** Blow Fish Encryption algorithm was implemented in FPGA using Verilog. It largely reduced time required to perform heavy calculations as compared to CPU.
Experience	**1. Maxense Innovation (Internee)** 2022-04~ Present Working on the development of low-power architecture for TDDI for mobile and smart-watch. The responsibilities include digital design verification, low power design development and power analysis of different modules of TDDI. **2. Damo Technology (Internee)** 2021-07~ 2022-04 Worked on the development of low-power architecture for TDDI for mobile and smart-watch. Moreover, responsibilities included verification and power analysis of different modules of TDDI. **3. Research Assistant** 2016-04 ~ 2016-07 Worked as research assistant for the project of “Integration of design thinking and TRIZ for prospective engineers”. The basic

	responsibilities included data collection, analysis and conducting sessions with research participants. 4. **Research Assistant cum Teaching Assistant** 2016-01~ 2016-03 The basic responsibilities included managing class and conducting activities in "Developing Professional Skills". The research responsibilities included the research on the change of behavior of students through the course by analyzing the data through qualitative research.
Internship	1. **Innovative design thinking** 2015-06~ 2015-08 This internship included courses on innovative design thinking process and TRIZ (a tool for problem solving). The project of this internship was redesigning of final year project lab.
Honors & Awards	1. Awarded full scholarship by National Central University, Taiwan, for Master and PhD 2. Awarded 90% scholarship by Namal College, Pakistan 3. Qualified for Quarterfinals in Robosprint Competition 2013 4. Served as the general secretary of Students Welfare Association Mianwali (SWAMI) 5. Selected as member of Namal Society for Social Impact
Publications	**1. M. A. Hussain**, S. A. Huang and T. H. Tsai, " Learning with Sharing: An Edge-optimized Incremental Learning Method for Deep Neural Networks," in *IEEE Transactions on Emerging Topics in Computing*, 2022. **2. M. A. Hussain**, L. C. Lee, and T. H. Tsai, " An Efficient Incremental Learning Algorithm for Sound Classification," in *IEEE Multimedia*, 2022. **3. M. A. Hussain**, L. C. Lee, and T. H. Tsai, " An Area-Efficient and High Throughput Hardware Implementation of Exponent Function," in *IEEE ISCAS*, 2022. **4. M. A. Hussain** and T. H. Tsai, "Memory Access Optimization for On-Chip Transfer Learning," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2021. **5. M. A. Hussain** and T. Tsai, "An Efficient and Fast Softmax Hardware Architecture (EFSHA) for Deep Neural Networks," in *IEEE AICAS*, Online, 2021. **6.** T. H. Tsai and **M. A. Hussain**, "VLSI Implementation of Lossless ECG Compression Algorithm for Low Power Devices," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2020. **7.** T. Tsai, C. Huang, C. Chang and **M. A. Hussain**, "Design of Wireless Vision Sensor Network for Smart Home," in *IEEE Access*, vol. 8, pp. 60455-60467, 2020. **8.** I. Althamary, **M. A. Hussain**, Y. H. Li, "An Improved Framework of

	Accurate Iris Segmentation under Relaxed Imaging Constraints using Total Variation Model", in *Conference on Computer Vision and Image Processing*, Taitung, Taiwan, 2019. **9.** T. H. Tsai, **M. A. Hussain**, P. Hao, "VLSI Implementation of ECG Compression Algorithm using Golomb Rice Coding", in *IEEE ICEE-Taiwan*, Taichung, Taiwan, 2018. ***(Best Paper Award)*** **10. M. A. Hussain** and R. Badar, "FPGA Based Implementation Scenarios of TEA Block Cipher," in *IEEE FIT*, Islamabad, Pakistan, 2015. **11.** M. Khan, **M. A. Hussain**, K. Chaudry, U. Tauseef, S. Nawaz, and R. Jawad, "A Bi-directional Prototype Mobile Robot to Experiment Light Scale Object-Transportation Schemes", in *IEEE ICET*, Islamabad, Pakistan, 2014.
Patents	1. U.S. Patent 17406458 "Device, Memory Access Method And Non-Volatile Storage Medium," December, 2022. 2. Taiwan Patent I769875, "深度學習網路裝置、其使用的記憶體存取方法與非揮發性儲存媒介," July, 2022.
Volunteer Work	**1. Flood relief activities in 2015** Volunteered for flood relief activities in different areas of Mianwali with Imran Khan Foundation. It included survey of affected area, distribution of aid and data entry of different people.
Extra-curricular activities	Gymnasium, Cooking
References	**1. Tsung-Han Tsai** Professor, Dept. of Electrical Engineering, National Central University, Taiwan. Email: han@ee.ncu.edu.tw Contact number: +886-03-422-7151 ext: 34472 **2. Yung-Hui Li** Director AI Research, Foxconn Corporation Email: yunghui@gmail.com